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EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 4/5/04, 4/26/04, 6/28/04.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 37-53 and 55-58 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 37-53 and 55-58 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Final Action

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named inventor is: WOHL
3. Applicant's Amendment was received 4/5/04, providing Remarks, but without compliant claims.
4. Applicant's Amendment was received 4/26/04, providing compliant claims, but non-responsive with respect to 35 USC 102(f).
5. Applicant's Amendment was received 6/28/04, addressing the 35 USC 102(f) issues.
6. This office action addresses the above three amendments.
7. Applicant's amendments cancelled claim 54, and amended claims 37, 38, 40, 42, 45, 47-53 and 55.
8. Thus, claims 37-53 and 55-58 are pending. The independent claims are: 37, 51, 53, and 55.
9. The US filing date is 7/23/99, and no earlier priority is claimed.

Index of Prior Art and Dictionaries

10. **Cheng** refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.
11. **Beausang'771** refers to US Patent 5,696,771.
12. **"Using Verilog Simulation Libraries for ATPG"** refers to "Using Verilog Simulation Libraries for ATPG", 0-7803-5753-1/99 1999 IEEE, by Peter Wohl, and John Waicukauski (Publication date 28-30 Sept. 1999).
13. **"Testing "untestable" faults in three-state circuits"** refers to "Testing "untestable" faults in three-state circuits" by Wohl et al, 0-8-86-7304-4/96, 1996, IEEE pages 324-333.
14. **Tucker** refers to "The Computer Science and Engineering Handbook", by Allen B. Tucker, CRC Press, ISBN: 0-8493-2909-4, 1996, pages 450-453.
15. **Smith** refers to "HDL Chip Design" by Douglas J. Smith, 1996, Ninth printing 2001 minor updates, ISBN 0-9651934-3-8, pages 38-40.

16. **MS Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
17. **McGraw-Hill Dictionary** refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., 2003, ISBN 0-07-042313-X.
18. **IEEE Dictionary** refers to The Authoritative Dictionary of IEEE Standards and Terms, Seventh Edition, by IEEE Press, ISBN 0-7381-2601-2, 2000.

Definitions

19. **"Associative memory"** is defined as "A type of memory whose locations are identified by their contents or by a part of their contents, rather than by their names or positions. Synonyms: search memory, content addressable storage" by IEEE Dictionary. Note that Tucker page 450-453 states "The cache memory is associative, or content-addressable. In an associative memory, the address of a memory location is stored, along with its content. Rather than reading data directly from a memory location, the cache is given an address and responds by providing data which may or may not be the data requested. When a cache miss occurs, the memory access is then performed with respect to the backing storage, and the cache is updated to include the new data."
20. **"Automatic test pattern generator (ATPG)"** as "Any tool that generates test information for a device based on structural analysis of the device", by IEEE Dictionary.
21. "**Content addressable memory**" (CAM) is defined as "See: associative memory" by IEEE Dictionary.
22. "**Logical**" is defined as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values… Boolean algebra", by MS Dictionary.
23. **"Primitive"** is defined as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program", by McGraw-Hill Dictionary.
24. **"Primitive"** is defined as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants", by MS Dictionary.
25. "**Random access memory"** (RAM) is defined as "(1) A memory that permits access to any of its address locations in any desired sequence with similar access time to each location (adapted from IEC 748-2). Note: The term RAM, as commonly used, denotes a read/write

memory with unlimited data rewrite capability and equal read and write times." by IEEE Dictionary.

Applicant's Remarks received 6/28/2004

26. Applicant persuasively asserts that inventor Timothy G. Hunkler contributed to pending claims 51-53 and 55-58. Thus the prior 35 USC 102(f) rejections are withdrawn.

Applicant's Remarks received 4/5/2004

27. 35 USC 101 STATUTORY SUBJECT MATTER-WITHDRAWN. The prior 35 USC 101 rejections are withdrawn due to Applicant's amendments to claims, and assertions at Remarks pages 8-9.
28. 35 USC 102 AND 35 USC 103-WITHDRAWN. PUBLICATION DATE OF "USING VERILOG SIMULATION LIBRARIES FOR ATPG". Applicant Remarks page 10 asserts that "Applicants submit herewith a Call for Papers for the International Test Conference in 1999… the International Test Conference started on September 28, 1999". The instant patent application was filed 7/23/99. Thus, Applicant asserts that the publication "Using Verilog Simulation Libraries for ATPG" is not prior art with respect to the instant application.
29. Note that the bottom left of said publication states "0-7803-5753-1/99 $10 (c) 1999 IEEE". The Examiner previously interpreted this statement as a publication date of 1/99.
30. However, it appears that the Examiner's interpretation was not correct. The IEEE abstract states **"Meeting Date: 09/28/1999 - 09/30/1999 Publication Date: 28-30 Sept. 1999".** Thus, the Applicant is correct that said paper is not prior art. The prior 35 USC 102(a) and 35 USC 103 rejections are thus withdrawn. The Examiner regrets any inconvenience caused by this misinterpretation.
31. 35 USC 112 ENABLEMENT AND INDEFINITENESS-WITHDRAWN. Applicant persuasively asserts that "A coupled to B" does not necessarily mean that the signal(s) flow from A to B. However, the point is that the term "coupled to" is not clear regarding the logical relationship. As a default rule (or rule of thumb), one of ordinary skill in the art may begin interpretation by assuming that "A coupled to B coupled to C" means that the logical signals flow from A to B to C. Most importantly, the apparent feedback/circular loop discussed in paragraph 33 of the prior office action was not reflected in the specification. Applicant has clarified the relevant claim language through amendments.

32. ADDITIONAL DRAWINGS REQUIRED-WITHDRAWN. Applicant asserts that the instant FIGs 6A and 10 (for example) correspond to the present claims, and that no additional drawings are needed. Due to the amendments to the claims, the requirement for additional drawings is withdrawn.

33. 35 USC 102(f) INVENTORSHIP-WITHDRAWN. The 35 USC 102(f) rejections are withdrawn due to Applicant's assertions in Remarks of 6/28/04.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.

36. Claims 37-53 and 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of "Testing "untestable" faults in three-state circuits".

37. Independent claim 37 is a "memory model" claim with 5 limitations, numbered by the Examiner for clarity.

38. [1]-"**a memory primitive** comprising a write address port, a write data port, and an output port"

39. [2]-"**a read data port primitive** comprising a read data port for coupling to the output port of the memory primitive, a read address port, and an output port"

40. [3]-"**an address bus primitive** comprising an output port for coupling to the write address port of the memory primitive and the read address port of the read data port primitive"

41. [4]-"**a data bus primitive comprising an output port** for coupling to the write data port of the memory primitive"

42. [5]-**“a plurality of memory out primitives,** each memory out primitive comprising an input port for coupling to the output port of the read data port primitive”
43. The above 5 limitations are disclosed by Beausang ‘771 at column 1 line 53-67 “components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology dependent mapped netlist”, and FIG 1 element 230 “CELL LIBRARY”, and FIG 8 element 655 “ATPG AND FORMAT”, and Column 14 line 40 “logical primitives”, and FIG 8 element 660 “TEST VECTORS”, and FIG 9 element 790 “VERIFY DESIGN TO HDL”, and FIG 8 element 605 “HDL DESCRIPTION”. Note that the column 1 line 55 term “latches and D-flip flops” disclose memory primitives. Further note that column line 56 “and their interconnections” discloses address bus and data bus.
44. In claim 38, there are 4 limitations:
45. [1] **“a set input port”**
46. [2] **“a reset port”**
47. [3] **“a write_clock port”**
48. [4] **“a write_enable port”**
49. The above 4 limitations are disclosed by Beausang ‘771 at column 1 line 53-67 “components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology dependent mapped netlist”, and FIG 1 element 230 “CELL LIBRARY”, and FIG 8 element 655 “ATPG AND FORMAT”, and Column 14 line 40 “logical primitives”, and FIG 8 element 660 “TEST VECTORS”, and FIG 9 element 790 “VERIFY DESIGN TO HDL”, and FIG 8 element 605 “HDL DESCRIPTION”.
50. In claim 39, **“the read data port primitive represents a read port functionality of the memory”** is disclosed by Beausang ‘771 at column 1 line 53-67 “components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology

dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

51. In claim 40, **"wherein a dimension of the output port of the read data port corresponds to a data dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
52. In claim 41, **"the address bus primitive represents an address functionality of a memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
53. In claim 42, **"the address bus primitive includes: a plurality of input ports corresponding to an address dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST

VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

54. In claim 43, "**the address bus primitive** further includes an attribute indicating whether an incoming address is encoded or decoded" is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

55. In claim 44, **"the data bus primitive represents a data bus functionality of the memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

56. In claim 45, **"a plurality of input ports corresponding to a data dimension of the memory primitive"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

57. <u>In claim 46,</u> **"each memory out primitive represents a simulated value storage functionality of the memory"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
58. <u>In claim 47,</u> **"an output port"** is disclosed by Beausang '771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
59. <u>In claim 48,</u> **"a plurality of tristate drivers can be coupled to the output ports of the memory out primitives, thereby representing an attribute of the read data port primitive"** is disclosed by "Testing "untestable" faults in three-state circuits" by Wohl et al, at Abstract "tristate... test generation techniques".
60. <u>In claim 49,</u> **"a plurality of edge-triggered registers can be coupled to the output ports of the memory primitives, thereby representing an attribute of the read data port primitive"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8

element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

61. In claim 50, **"input ports of a plurality of tristate drivers can be coupled to the output ports of the plurality of edge-triggered registers, thereby representing an attribute of the read data port primitive"** is disclosed by "Testing "untestable" faults in three-state circuits" by Wohl et al, at Abstract "tristate… test generation techniques".
62. Claim 51 is an independent "content addressable memory model" claim with 5 limitations:
63. [1]-**"a memory primitive including an output port"**
64. [2]-**"a compare port primitive including a data port for coupling to the output port of the memory primitive, a data bus port, and an output port"**
65. [3]-**"a data bus primitive for coupling to the memory primitive"**
66. [4]-**"a plurality of memory out primitives, each memory out primitive for coupling to the compare port primitive"**
67. [5]-**"an address bus primitive including input ports for coupling the output ports of a set of the memory output primitives"**
68. The above 5 limitations are disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".
69. In claim 52, "a compare enable port for receiving a compare signal" is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST

VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

70. Claim 53 is an independent "combined CAM and RAM model" with 11 limitations:
71. [1]-**"a first memory primitive including an output port"**
72. [2]-**"a data bus primitive including an output port"**
73. [3]-**"a compare port primitive... comprising ; a compare enable port"**
74. [4]-**"a data bus port for coupling to the output port of the first memory primitive"**
75. [5]-**"a data port for coupling to the output port of the first memory primitive"**
76. [6]-**"a first plurality of memory output primitives, each memory output primitive including an output port and an input port for coupling to the output port of the compare port primitive"**
77. [7]-**"an address bus primitive including an output port and an input port for coupling to the output port of the compare port primitive"**
78. [8]-**"an address bus primitive including an output port and input ports for coupling to output ports of a first subset of the first plurality of memory output primitives"**
79. [9]-**"a second memory primitive including an output port"**
80. [10]-**"a read data primitive including a first input port for coupling to the output port of the second memory primitive, a second input port for coupling to an output port of the address bus primitive, and a third input port for coupling to the output ports of a second subset of the plurality of memory output primitives"**
81. [11]-**"a second plurality of memory output primitives, each memory output primitive including an input port for coupling to an output port of the read data port primitive"**
82. The above 11 limitations are disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

83. <u>Claim 54</u> has been cancelled.

84. <u>In claim 55,</u> **"a plurality of primitives, each primitive representing a defined functionality of a memory"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

85. <u>In claim 56,</u> **"each primitive usable by the ATPG tool is configured based on a subset of behavioral hardware description language (HDL) usable by the simulation tool"** disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION".

86. <u>In claim 57,</u> **"the behavioral HDL includes Verilog"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design... netlist of generic primitive cells... then applies a particular cell library... to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION". Note that Verilog is one of the two most common HDL languages: Verilog and VHDL.

87. In claim 58, **"the subset of behavioral HDL can directly map to the plurality of primitives"** is disclosed by Beausang'771 at column 1 line 53-67 "components of a netllist can include primitive cells such as full-adders, NAND gates, NOR gates, XOR gates latches and D-flip flops, etc. and their interconnections used to form a custom design… netlist of generic primitive cells… then applies a particular cell library… to generate a technology dependent mapped netlist", and FIG 1 element 230 "CELL LIBRARY", and FIG 8 element 655 "ATPG AND FORMAT", and Column 14 line 40 "logical primitives", and FIG 8 element 660 "TEST VECTORS", and FIG 9 element 790 "VERIFY DESIGN TO HDL", and FIG 8 element 605 "HDL DESCRIPTION". Note that Verilog is one of the two most common HDL languages: Verilog and VHDL.
88. **MOTIVATION.** At the time of the invention, one of ordinary skill in the art would have been motivated to use "Testing "untestable" faults in three-state circuits" by Wohl et al to modify Beausang'771 in order to "increased test coverage… while decreasing CPU time" according to the Abstract of "Testing "untestable" faults in three-state circuits" by Wohl et al.

Response to Amendments or new IDS-FINAL OFFICE ACTION

89. Applicant's amendments or new IDS necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

90. All pending claims stand rejected under 35 USC 103.

Communication

91. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER